32.   (New) The computer-readable medium of claim 21, wherein the indication reflects a number of cycles the selected thread was running in a portion of the program that is active when it is determined the selected thread is running.

33.   (New) The computer-readable medium of claim 24, wherein the time-profiling information includes a cost indicator that reflects a number of cycles the selected thread was running in the portion of the program that is active when it is determined the selected thread is running.

REMARKS

In the Office Action dated August 15, 2002, the Examiner rejected claims 1-6, 8-22, 24, and 25 under 35 U.S.C. § 102(e) as being anticipated by Agrawal et al. (U.S. Patent No. 5,768,500).

By this amendment, Applicant has added new claims 26-33 to recite further aspects related to the present invention. Based on the following remarks, Applicant respectfully traverses the rejection of claims 1-6, 8-22, 24, and 25 under 35 U.S.C. § 102(e) because Agrawal et al. does not teach every recitation of these claims.

Agrawal et al. teaches a system for profiling memory system performance by sampling state information during periods of interrupt. The system monitors, for example, cache misses through an event detection circuit 102. When a certain number of cache misses are detected, a counter circuit provides a pulse signal to an interrupt
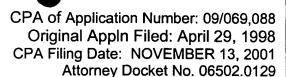
generator that causes a system bus interrupt to occur. Based on the interrupt, the system may record system state information to a profiling buffer. A user-level process periodically copies the profiling buffer to a file. Subsequently, "post mortem" tools synthesize cache miss profiles on a per-process basis. Alternatively, the system may perform user-level profiling that allows an interrupt handler to determine, following an interrupt, whether an executing processes has opened a sampling process. If so, the handler posts a signal to the process and when the program is to be resumed, the system's kernel allows the interrupted process to be restarted in a registered signal handler. The handler records process state information returns control to the process' previously executing thread of operation.

In contrast, claim 1 recites a combination of steps including periodically interrupting execution of all of the threads, determining whether register data corresponding to a selected thread has changed from a previous interrupt of all of the threads of a program, and providing an indication of the change for the selected thread. Agrawal et al. does not teach this combination, including, among other things, the step of determining whether register data has changed and providing an indication of the change. Instead, the wide-profiling procedure described by Agrawal et al., and cited by the Examiner, simply records sampled state information each time a sampling interrupt occurs. This profiling procedure does not determine whether register data for a selected thread has changed form a previous interrupt. In fact, Agrawal et al. teaches that the wide-sampling process requires that the recorded state information be copied to

a file that is analyzed offline ("post mortem") for review of cache misses (see Agrawal et al., col. 10, lines 22-42).

Further, the "User Level Sampling in Cpprof" case study described in col. 13, lines 8-62 of Agrawal et al., and cited by the Examiner, does not teach the above mentioned recitations of claim 1. Instead, this exemplary case study refers to a process of profiling real time and data stall time (i.e., interrupt time) data using the user-level sampling techniques discussed above. The only comparing functions performed by Agrawal et al. in this case study are associated with the performance of sorting routines (e.g., the time it takes to perform a particular type of sort function) (see Agrawal et al., col. 13, lines 8-62 and Table 2). Agrawal et al. does not teach determining whether register data has changed from a previous interrupt of a program executing multiple threads, as recited in claim 1.

Moreover, Agrawal et al. does not teach providing an indication of the determined change, as recited in claim 1. The interrupt status bits, referred to by the Examiner, reflect which monitored event caused an interrupt. The events are associated with monitored features of the processing system under analysis, such as a cache miss. For example, in Agrawal et al., a monitor circuit sends a trigger signal to downcounter 104 each time a monitored event is detected, such a primary or secondary level cache miss. An interrupt is generated by a comparator, which compares a threshold value to a current count value of the downcounter. The interrupt status bits merely indicate which of the monitored events (e.g., cache miss) caused the interrupt. Accordingly, Agrawal et al. does not provide an indication of a change of register data corresponding to a

selected thread, as recited in claim 1. In fact, this reference does not even compare register data from a previous interrupt, but instead merely compares count values to a threshold value stored in a comparator circuit.
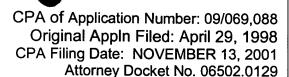
Because Agrawal et al. does not teach the recitations of claim 1, Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.

Claims 2-4 depend from claim 1. As explained, claim 1 is distinguishable from Agrawal et al. Accordingly, claims 2-4 are also distinguishable from this reference for at least the same reasons set forth for claim 1.

Further, Agrawal et al. does not teach comparing stored data corresponding to the selected thread with register information following a previous interrupt, as recited in claim 2. Instead, the reference teaches comparing a user specified value of a compare register with a read wait time counter to determine whether to execute an interrupt (see Agrawal et al., col. 16, lines 15-41). Accordingly, Agrawal et al. cannot teach the recitations of claim 2 because (1) the comparing function is associated with a counter value and not register data corresponding to a selected thread and (2) the comparing function is performed to determine when to execute an interrupt, thus is performed prior to an interrupt occurring.

Regarding claim 3, Agrawal et al. does not teach computing a value corresponding to the stored data recited in claim 2 and determining a relationship between the computed value and the previously stored register information. In fact,
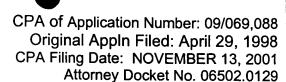
Applicant cannot ascertain where in the cited portion of Agrawal et al. (e.g., col. 16, lines 15-41), much less anywhere else in this reference, such steps are performed.

Regarding claim 4, Agrawal et al. does not teach updating a memory segment to reflect that the selected thread is running when it is determined that the computed value and the previously stored register value do not match, as recited in this claim. The counter bookkeeping process described by Agrawal et al. is associated with determining a cycle cost of a counting semaphore used to protect an update code (see Agrawal et al., col. 5, line 55 to col. 6, line 6). There is no disclosure or suggestion in this reference of updating a memory segment as recited in claim 4.

Because Agrawal et al. does not teach the additional recitations of claims 2-4, Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn and the claims allowed.

Claim 5 includes recitations similar to those of claims 1, 3 and/or 4 . As explained, claims 1, 3, and 4 are distinguishable from Agrawal et al. Accordingly, claim 5 is also distinguishable from this reference for at least the same reasons set forth for claims 1, 3, and/or 4. Further, the Examiner did not address all of the recitations of claim 5. For example, claim 5 recites a combination of steps including providing an indication corresponding to a portion of the program containing the selected thread. This step is not recited in claim 1 and was not addressed in the Office Action. Further, Agrawal et al. does not teach this recitation. Accordingly, because the Examiner failed to address, and Agrawal et al. does not teach every recitation of claim 5, Applicant

respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.
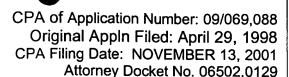
Claim 6 depends from claim 5. As explained, claim 5 is distinguishable from Agrawal et al. Accordingly, claim 6 is also distinguishable from this reference for at least the same reasons set forth for claim 5. Further, Agrawal et al. does not teach updating the previous register information based on the computed value, as recited in clam 6, and Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.

Regarding canceled claims 7 and 23, the Examiner rejected these claims on page 5, lines 3-5 of the outstanding Office Action. Because these claims were canceled in the response filed May 28, 2002, Applicant respectfully requests confirmation on the status of these claims in the next communication from the Examiner.

Claims 8, 9, 16, 17, 24, and 25 include recitations similar to those of claim 1. As explained, claim 1 is distinguishable from Agrawal et al. Accordingly, claims 8, 9, 16, 17, 24, and 25 are also distinguishable from this reference for at least the same reasons set forth for claim 1, and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn and the claims allowed.

Claims 10-12 depend from claim 9. As explained, claim 9 is distinguishable from Agrawal et al. Accordingly, claims 10-12 are also distinguishable from this reference for at least the same reasons set forth for claim 9 and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn and the claims allowed.
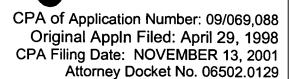
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Claim 13 includes recitations similar to those of claim 5. As explained, claim 5 is distinguishable from Agrawal et al. Accordingly, claim 13 is also distinguishable from this reference for at least the same reasons set forth for claim 5 and Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.

Claims 14 and 15 depend from claim 13. As explained, claim 13 is distinguishable from Agrawal et al. Accordingly, claims 14 and 15 are also distinguishable from this reference for at least the same reasons set forth for claim 13. Further, Agrawal et al. does not teach providing an indication corresponding to a portion of the program containing the selected thread, as recited in claim 15. Instead, the down counting and interrupt features disclosed in columns 9-10 of Agrawal et al. are related to triggering interrupts based on monitored events and not the provision of an indication of a portion of a program containing a selected thread. Because Agrawal et al. does not teach or even suggest the recitations of claims 14 and 15, Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn and the claims allowed.

Claims 18-20 depend from claim 13. As explained, claim 13 is distinguishable from Agrawal et al. Accordingly, claims 14 and 15 are also distinguishable from this reference for at least the same reasons set forth for claim 13, and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn and the claims allowed.

Claim 21 includes recitations similar to those of claim 5. As explained, claim 5 is distinguishable from Agrawal et al. Accordingly, claim 21 is also distinguishable from this reference for at least the same reasons set forth for claim 5, and Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.

Claim 22 depends from claim 21. As explained, claim 21 is distinguishable from Agrawal et al. Accordingly, claim 22 is also distinguishable from this reference for at least the same reasons set forth for claim 21, and Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 102(e) be withdrawn and the claim allowed.

Regarding claims 26-33, Agrawal et al. does not teach or suggest assigning a cost indicator to an identified portion of the program that is active when it is determined that the selected thread is running or a cost indicator that reflects a number of cycles the selected thread was running in the identified portion of the program, as recited in these claims.

Because Agrawal et al. does not teach the recitations of claims 1-6, 8-22, and 24-33, Applicants respectfully requests that the rejection of claims 1-6, 8-22, 24, and 25 under 35 U.S.C. § 102(e) be withdrawn and claims 1-6, 8-22, and 24-33 allowed.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: October 31, 2002

By:_____

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